

DESCRIPTION

VK4101 is an 8-character, 14-segment intelligent module designed to communicate with microprocessor through an 8-bit serial interface.

FEATURES

- Low power consumption CMOS technology.
- Compact design and easy panel mounting.
- Built-in 14-segment ASCII alphanumeric decoder.
- Two 32x4 static RAM for display data and blinking data storage.
- An intelligent quadruplex driver display module.
- positive or negative mode option.
- 14.00mm (0.55inch) alphanumeric Character height.
- +5V single power supply.
- Highly reliable and uniform LED backlight.
- Serial data input.

OPERATING SPECIFICATIONS

Operating Temperature -10°C to +70°C
 Storage Temperature -30°C to +85°C
 Operating Relative Humidity 90% max

ORDERING INFORMATION

VK4101 Positive mode LCD
 VK4101L Positive mode LCD with backlighting
 VK4101N Negative mode LCD with backlighting

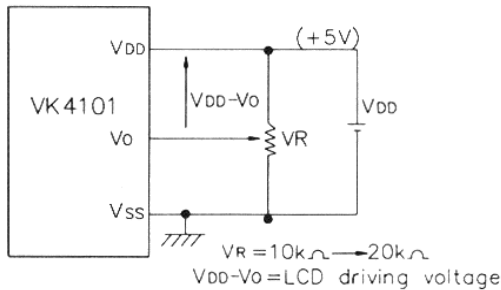
ELECTRICAL CHARACTERISTICS (Ta = +25°C, VDD = 5V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	VDD		3.0	5.0	5.5	V
Current consumption	IDD			200		μA
Input high voltage	VIH		0.7VDD		VDD	V
Input low voltage	VIL		0		0.3VDD	V
Output high voltage	VOH	Output current = -10 μA	VDD - 0.5			V
Output low voltage	VOL	Output current = 100 μA			0.5	V
Power supply for LCD drive	VDD - VO	Ta = 0°C		4.7		V
		Ta = 25°C		4.5		V
		Ta = 50°C		4.0		V
LED forward voltage	VLED	L+ If = 80mA	4.5	5.0	5.5	V
Peak spectrum	λ	If = 80mA		565		nm
SCK cycle	tcyk		900			ns
SCK high pulse width	tWHK		400			ns
SCK low pulse width	tWLK		400			ns
SI set-up time to SCK ↑	tisk		100			ns
SI hold time after to SCK ↓	tihk		200			ns
C/D set-up time to 8th. SCK ↑	tDSK		9			μs
C/D hold time after 8th. SCK ↓	tDHK		1			μs
CS hold time after 8th. CLK ↑	tCHK		1			μs
CS pulse width low	tCWL		40			μs
CS pulse width high	tCWH		40			μs

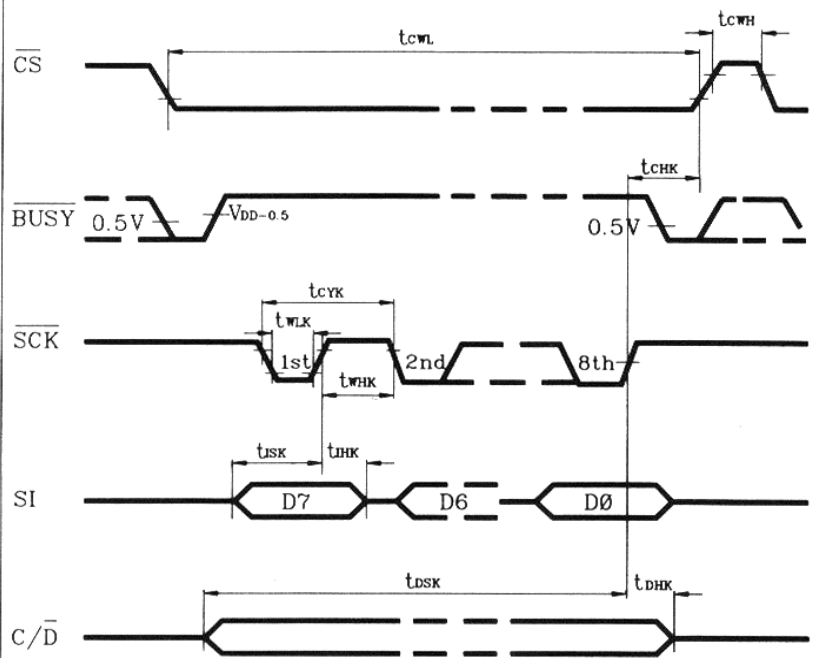
DEFINITION OF TERMINALS

PIN NO.	SYMBOL	FUNCTION
1	V _{SS}	Ground terminal
2	V _{DD}	Supply terminal
3	V _o	LCD driving voltage
4	SCK	Serial clock input
5	SI	Serial input
6	CS	Chip select input
7	BUSY	Busy output
8	C/D	Command/Data select
9	RESET	Reset Input
10	NC	No connection
11	L-	Terminal for backlighting with limiting resistor
12	L+	

POWER SUPPLY



TIMING DIAGRAM



DECODED DISPLAY RAM DATA 14-Segment Alphanumeric Data Decoder Character Set

Display byte (HEX)	Char.	Display RAM address				Display byte (HEX)	Char.	Display RAM address				Display byte (HEX)	Char.	Display RAM address				Display byte (HEX)	Char.	Display RAM address			
		n+3	n+2	n+1	n			n+3	n+2	n+1	n			n+3	n+2	n+1	n			n+3	n+2	n+1	n
A0	☒	0	0	0	0	B0	☒	4	7	E	2	C0	☒	A	7	C	0	D0	☒	2	3	6	4
A1		Invalid				B1	☒	0	6	0	0	C1	☒	2	7	6	4	D1	☒	0	7	E	8
A2		Invalid				B2	☒	2	3	C	4	C2	☒	8	7	8	5	D2	☒	2	3	6	C
A3		Invalid				B3	☒	2	7	8	4	C3	☒	0	1	E	0	D3	☒	1	5	8	4
A4		Invalid				B4	☒	2	6	2	4	C4	☒	8	7	8	1	D4	☒	8	1	0	1
A5		Invalid				B5	☒	2	5	A	4	C5	☒	2	1	E	4	D5	☒	0	6	E	0
A6		Invalid				B6	☒	2	5	E	4	C6	☒	2	1	6	4	D6	☒	4	0	6	2
A7	☒	0	0	0	2	B7	☒	0	7	0	0	C7	☒	0	5	E	4	D7	☒	4	6	6	8
A8	☒	0	0	0	A	B8	☒	2	7	E	4	C8	☒	2	6	6	4	D8	☒	5	0	0	A
A9	☒	5	0	0	0	B9	☒	2	7	A	4	C9	☒	8	1	8	1	D9	☒	9	0	0	2
AA	☒	F	0	0	F	BA		Invalid				CA	☒	0	6	C	0	DA	☒	4	1	8	2
AB	☒	A	0	0	5	BB		Invalid				CB	☒	2	0	6	A	DB		Invalid			
AC		Invalid				BC	☒	4	0	8	2	CC	☒	0	0	E	0	DC	☒	1	0	0	8
AD	☒	2	0	0	4	BD	☒	2	0	8	4	CD	☒	1	6	6	2	DD	☒	Invalid			
AE		Invalid				BE	☒	1	0	8	8	CE	☒	1	6	6	8	DE		Invalid			
AF	☒	4	0	0	2	BF		Invalid				CF	☒	0	7	E	0	DF		Invalid			