

PIN-OUT ASSIGNMENT

PIN NO.	SYMBOL	FUNCTION	LEVEL
1~4	UD0~UD3	Display data signal	H/L
5	CP	Data Shift	H→L
6	LP	Data Latch	H→L
7	M	Control signal for AC driving	H/L
8	FLM	Frame frequency (indicating the beginning of each display cycle)	H
9	DISPOFF	Blanking signal	High(ON) Low(OFF)
10	VDD	Power Supply for logic and LCD(+)	-
11	CONT-GND	Ground potential for contrast circuit	-
12	CONT-ADJ.	Contrast adjustment	-
13,14	GND	Ground potential for logic circuit	-
15	N.C.	-	-
16	AUDIO+	Audio input for buzzer	-
17	AUDIO-	Terminal of audio ground	-
18	N.C.	-	-
19	ELCNTL	EL backlight control signal	High(OFF) Low(ON)
20	ELGND	Ground potential for EL circuit	-

ABSOLUTE MAXIMUM RATING

NO.	PARAMETER	SYMBOL	MIN	MAX	UNIT
1.	Power supply for logic	VDD - VSS	0	7.0	V
2.	Input voltage	VI	VDD	VSS	V
3.	Operating temperature	Ta	0	50	°C
4.	Storage temperature	Tstg	-20	70	°C

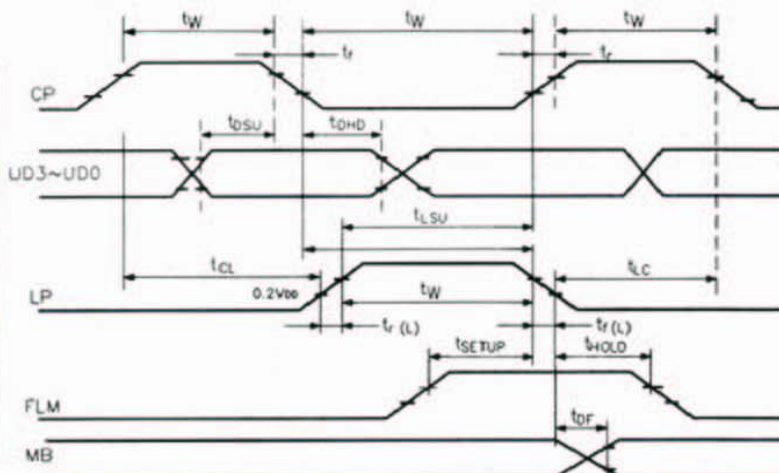
ELECTRICAL CHARACTERISTICS

(Ta = +25°C)

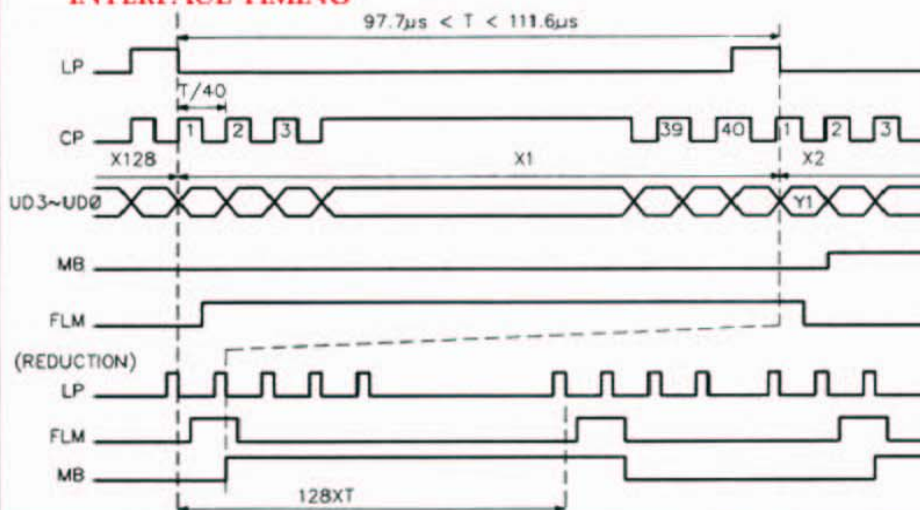
NO.	PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
1.	Supply voltage	VDD	-	4.5	5.0	5.5	V
2.	-Normal off mode Module current-Display off mode	IDD IDDSBY	VDD=5.0V DISPLAY OFF = '0'V	-	15 3	20	mA mA
3.	Module current during EL 'ON'	IDD	ELCNT='0'V	-	65	-	mA
4.	Input high voltage for logic	VIH	VDD=4.5V	3.15	-	-	V
5.	Input low voltage for logic	VIL	VDD=4.5V	-	-	1.0	V
6.	Audio input frequency	-	-	2	-	4	KHz
7.	EL control input signal	VELCNTL	-	0	-	VDD	V

INTERFACE TIMING

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Frequency for maximum clock	tCP	-	-	3.0	MHz
CP,LP pulse width	tW	125	-	-	nS
Rise, fall time	tr,tf	-	-	50	nS
Data set up time	tDSU	100	-	-	nS
Data hold time	tDHD	100	-	-	nS
CP → LP time	tCL	200	-	-	nS
LP set up time	tLC	125	-	-	nS
LP → CP time	tSETUP	200	-	-	nS
FLM set up time	tSETUP	100	-	-	nS
FLM hold time	tHOLD	100	-	-	nS
MB delay time	tDF	-	-	300	μS



INTERFACE TIMING



APPLICATION DIAGRAM

