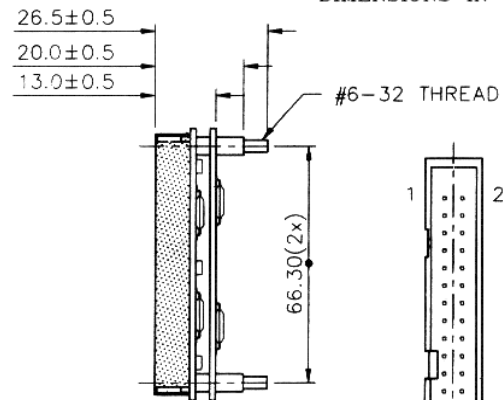
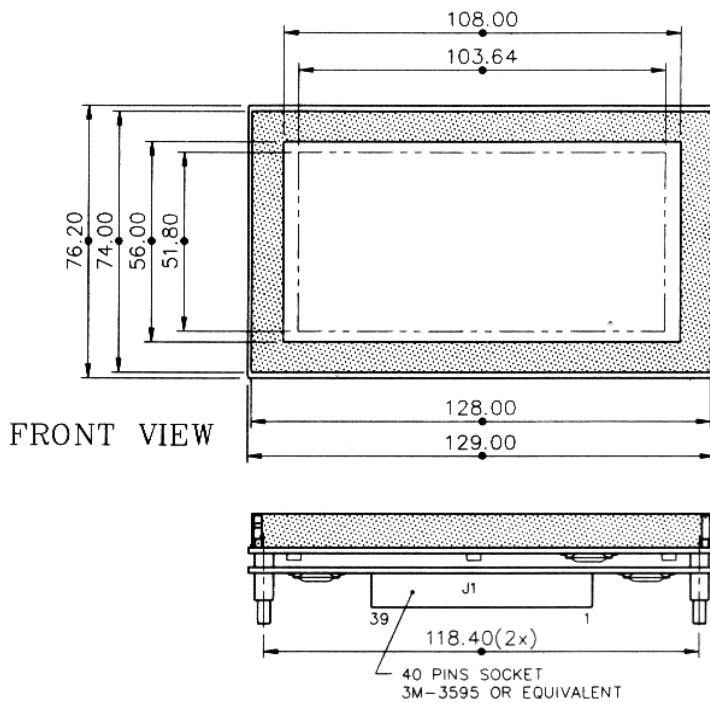
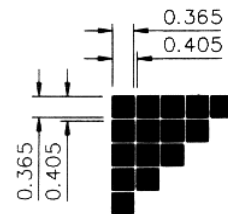


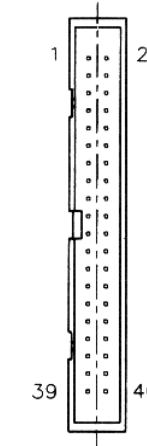
MODULE DIMENSIONS



SIDE VIEW

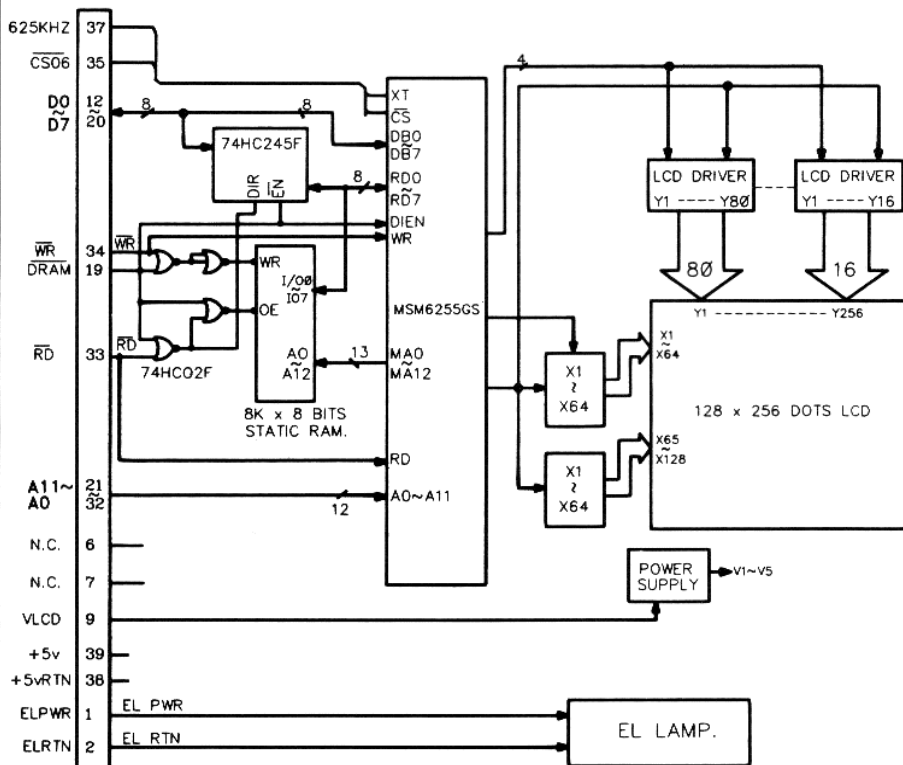


DIMENSIONS IN MM



TOP VIEW FOR J1

BLOCK DIAGRAM



PIN-OUT ASSIGNMENT

PIN NO.	SYMBOL	FUNCTION	INPUT/OUTPUT
1	ELPWR	Power Supply for EL panel	-
2	ELRTN	Ground potential for EL panel	-
3,4,5	N.C	-	-
6	N.C	-	-
7	N.C	-	-
8	N.C	-	-
9	VLCD	Operating voltage for LC driving(-)	-
10,11	N.C	-	-
12	D0	Data bus (LSB)	I/O
13	D2	Data bus	I/O
14	D1		
15	D4		
16	D3		
17	D6		
18	D5		
19	DRAM	Display enable signal. When this signal is H, display is enable.	INPUT
20	D7	Data bus (MSB)	I/O
21~32	A11~A0	Address bus	INPUT
33	RD	Read....Reading data is valid when RD=L	INPUT
34	WR	Write....Data is written when WR=L	INPUT
35	CS06	Chip enable	INPUT
36	N.C	-	-
37	625KHZ	External clock	INPUT
38	+5VRTN	Ground potential for logic circuit	-
39	+5V	Power supply for logic and LCD(+)	-
40	N.C	-	-

ABSOLUTE MAXIMUM RATING

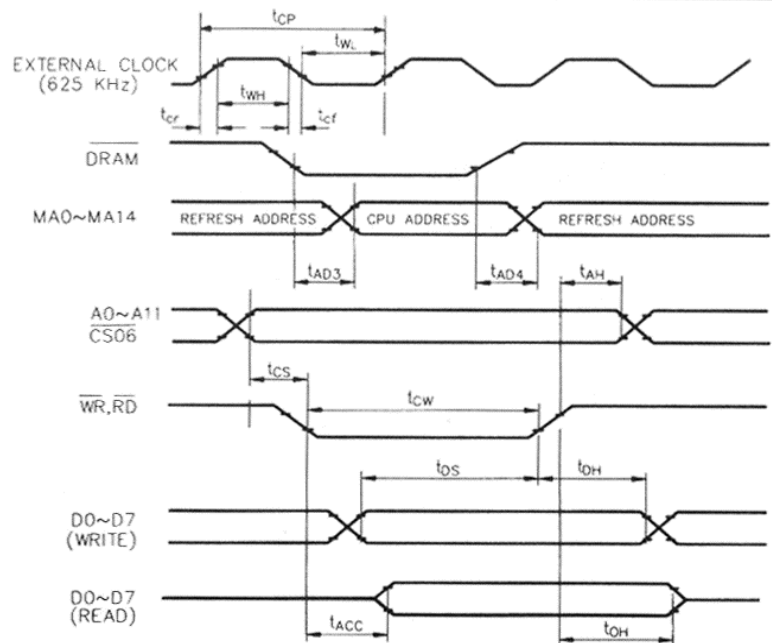
NO.	PARAMETER	SYMBOL	MIN	MAX	UNIT
1.	Power supply for logic	VDD - VSS	∅	7.0	V
2.	Power supply for LCD drive	VDD - VLCD	∅	22.0	V
3.	Input voltage	VI	VDD	VSS	V
4.	Operating temperature	To	0	50	°C
5.	Storage temperature	Tstg	-20	70	°C

ELECTRICAL CHARACTERISTICS (Ta = +25°C)

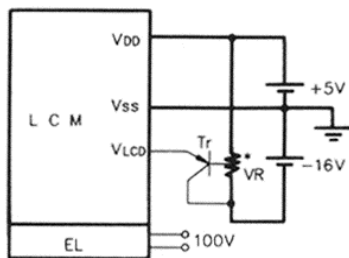
NO.	PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
1.	Supply voltage	VDD	-	4.5	5.0	5.5	V
2.	Module supply current	I _{OD}	VDD = 5.0V	-	-	17	mA
		I _{EE}	-	-	-	5	mA
3.	Operating voltage for LCD drive 1/128 duty (Recommended)	VDD - VLCD	--	-	18.6	-	V
4.	High level input voltage for logic	V _{IH}	VDD = 5.0V	0.7 VDD	-	VDD	V
5.	Low level input voltage for logic	V _{IL}	VDD = 5.0V	0	-	0.3 VDD	V
6.	EL AC Supply voltage	VEL	-	-	82.5V	-	VAC

INTERFACE TIMING

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
CPU address delay time	t _{AD3}	-	-	100	nS
Refresh address delay time	t _{AD4}	-	-	100	nS
Reset low level pulse width	t _{RES}	1	-	-	nS
Address bus CS set up time	t _{CS}	100	-	-	nS
RD,WR pulse width	t _{CW}	300	-	-	nS
Address hold time	t _{AH}	40	-	-	nS
Data set up time	t _{DS}	200	-	-	nS
Data hold time	t _{DH}	40	-	-	nS
Output disable time	t _{OH}	0	-	40	nS
Access time	t _{ACC}	-	-	200	nS
External clock Cycle time	t _{CP}	180	-	-	nS
Clock rising/falling time	t _{cr} / t _{cf}	-	-	10	nS



POWER SUPPLY



VOLTAGE SEQUENCING

